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Design of a Low Power and Area Efficient Flip Flop With Embedded Logic Module

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Abstract: *As number of modules per chip is increasing, number of transistors in a chip increases resulting in increase in area and power dissipation. Area and power dissipation problems can be most effectively addressed if the basic building blocks of the circuit are designed for lower power dissipation and occupy less space. Flip-Flop, which is basic building block, plays a major role in design of complex systems. From the open literature, Semi Dynamic Flip-Flop (SDFF) and Dual Dynamic Flip-Flops (DDFF) are classic structures which are efficient for incorporating complex logic functions. In this paper, a new low power and area efficient flip-flop with Embedded Logic Module (ELM) is proposed. The proposed Flip-Flop reduces 50% to 60% of power dissipation as compared to conventional flip-flops and delay up to 86% is also reduced. Serial in Parallel out (SIPO) shift register is designed with the proposed flip-flop which exhibit low power dissipation. The simulations are done in MENTOR GRAPHICS, Schematic editor, Generic GDK, 130nm technology.*

Index terms: *SDFF, DDFF, high speed, low power, embedded logic.*

I. Introduction

Sequential logic circuits, such as registers, memory elements, counters etc., are heavily used in the implementation of VLSI circuits. As VLSI circuits continue to evolve and technologies progresses, the level of integration is increased and higher clock speed is achieved. Higher clock speeds, increased levels of integration and technology scaling are causing unabated increases in power consumption. As a result, low power consumption is becoming a critical issue for modern VLSI circuits. Furthermore, power dissipation, dynamic and static, has become a limiting factor for transistor performance, long term device reliability, and increasing integration.

Flip-flop is a data storage element. The operation of the flip-flops is done by its clock frequency. When multistage flip-flop is operated with respect to clock frequency, it processes with high clock switching activity and then increases time latency. Therefore it affects the speed and energy performance of the circuit. Various classes of flip-flops have been proposed to achieve high-speed and low-energy operation. From the open literature, Semi Dynamic Flip-Flop (SDFF) and Dual Dynamic Flip-Flops (DDFF) are classic structures which are efficient for incorporating complex logic functions [1].To achieve low power dissipation along with area efficiency, a new low power and low area Flip-Flop with Embedded Logic Module (ELM) is proposed and is compared with the conventional Flip-Flops.

II. Power Dissipation

Power dissipation is recognized as a critical parameter in modern VLSI design field. The design of portable devices requires consideration for peak power consumption to ensure reliability and proper operation. However, the time averaged power is often more critical as it is linearly related to the battery life. There are four sources of power dissipation in digital CMOS circuits: switching power, short-circuit power, leakage power and static power. The following equation describes these four components of power:

$$P_{avg} = \alpha C L V_{dd} V_{sfck} + I_{sc} V_{dd} + I_{leakage} V_{dd} + I_{static} V_{dd} \quad (1)$$

Here $P_{static} = \alpha C L V_{dd} V_{sfck}$,
$P_{dynamic} = I_{sc} V_{dd}$,
$P_{leakage} = I_{sc} V_{dd}$
and $P_{short\text{-}circuit} = I_{static} V_{dd}$

III. Conventional Flip-Flop

Architectures

A. Semi Dynamicflip-Flop (Sdff)

The dynamic flip-flops include the modern high performance flip-flops. They are divided into purely dynamic designs and pseudo-dynamic structures. The distinctive performance improvements are achieved by having an internal precharge structure and a static output. They are called as the semi-dynamic or hybrid structures because of having a dynamic frontend and a static output. SDFF suffers from large power consumption because of the large CLK load as well as the large precharge capacitance [1, 2]. This design is efficient for incorporating complex logic functions effectively as shown in fig 1.

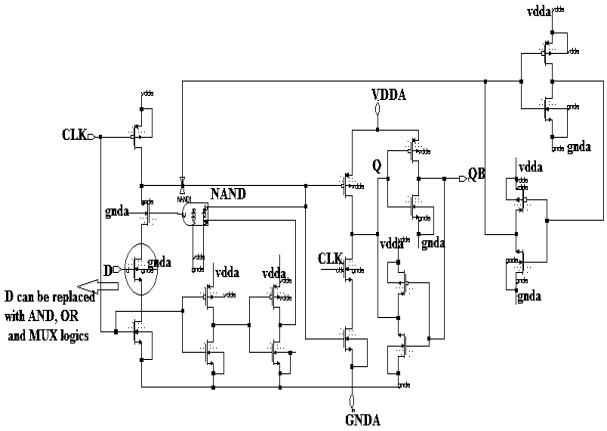

Fig 1: Semi Dynamic Flip Flop (SDFF).

B. Dual Dynamic Flip-Flop (Ddff)

The dual dynamic pulsed flip flop (DDFF) architecture acts as both static and dynamic circuit. The operation of DDFF is based on dynamic logic principles [3]. The flip flop operation can be divided into two phases. First the evaluation phase, when the clock (CLK) signal is high and second the precharge phase, when the clock (CLK) signal is low. The actual latching takes place during the 1-1 overlap of CLK and CLKB during the evaluation phase. If the data input (D) is high prior to this overlap period, node X1 is now discharged through M6. This switches the logic state of the cross coupled inverter pair INV1-2 causing node X1B to go high and output QB to discharge through M14. The low level at the node X1 is continued by the inverter pair INV1-2 for the rest of the evaluation phase where no latching occurs. Thus, node X2 is now held high throughout the evaluation phase by the PMOS transistor M11. As

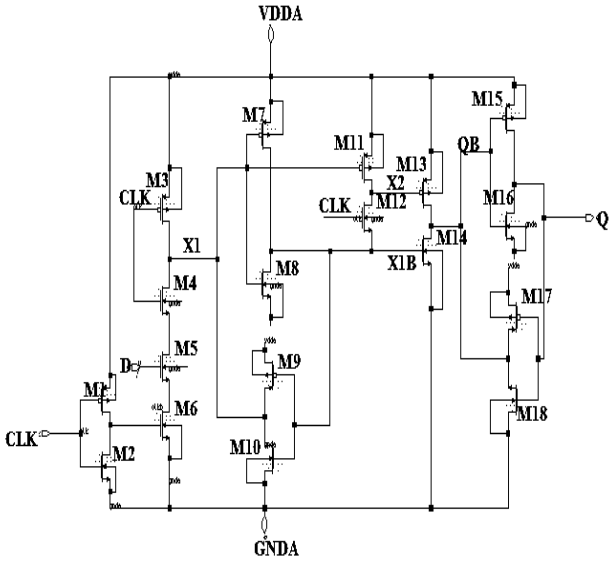

Fig 2: Dual Dynamic Flip Flop (DDFF).

the CLK signal falls low, the circuit enters into the precharge phase and node X1 is pulled high through M3, switching the logic state of INV1-2. During this period of operation node X2 is not actively driven by any transistor, it stores the charge dynamically [4, 5]. The outputs at node QB and maintain their voltage levels through the inverter pair INV3-4 as shown in Fig 2.

If data input D is zero prior to the overlap period, the node X1 remains high and the node X2 is pulled low through NMOS transistor M12 as the CLK signal goes high [6,7]. Thus, the node QB is charged to high through PMOS transistor M13 and NMOS transistor M14 is held off. At the end of the evaluation phase, as the CLK falls to low, the node Y1 remains high and Y2 stores the charge dynamically. This design exhibits negative setup time since the short transparency period defined by the 1–1 overlap of CLK and CLKB allows the data to be sampled even after the rising edge of the CLK before CLKB falls low. Node X1 undergoes charge sharing when the clock (CLK) makes a low to high transition while data (D) is held low. This results in a momentary fall in voltage at node Y1, but the inverter pair INV1-2 should be skewed properly such that it has a switching threshold well below the worst case voltage drop at node X1 due to charge sharing. The timing diagram of DDFF shows that node X2 retains the charge level during the precharge phase when it is not driven by any transistor. One of the major drawbacks of this design is the redundant precharge at node X2 and X1 for data patterns containing more number of 0s and 1s, respectively.

In order to overcome the drawbacks occurred in SDFF and DDFF a new low power and area efficient flip-flop with Embedded Logic Module (ELM) is proposed. The proposed flip flop is designed in such a way that it comes with the reduced area due to minimum number of transistors used for the design. The basic concept behind this structure comes from the overlap based cell and the DDFF design mentioned above. The power dissipation of this flip-flop design is lower than the existing flip-flop designs as shown in Fig 3.

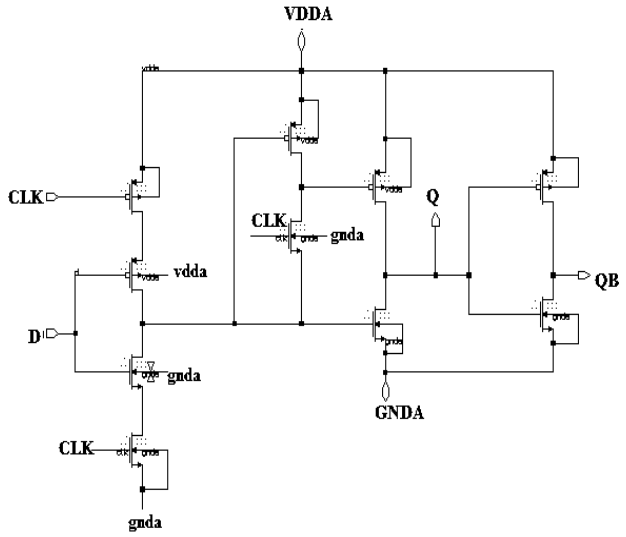

Fig 3: Proposed Flip Flop

A part from this the above discussed SDFF, DDFF and proposed flip-flops are efficient for Embedded Logic Module (ELM). Several functions have been embedded into the dual dynamic flip flop (DDFF) in order to analyze the performance of the structure in terms of speed and power [8, 9]. Since SDFF is considered as basic circuit for comparison, it was also simulated under similar conditions when embedded with the same functions. SDFF design has a fast non-inverting output and a slow inverting output, whereas the DDFF design has a fast inverting output and a slow non-inverting output.

IV. Embedded Logic Module (Elm):

In order to have a fair comparison of delay, area and power dissipation for SDFF, DDFF and proposed flip-flop designs. AND, OR functions and a two-input multiplexer implementing the function A.SELA+B.SELB were embedded into three designs by replacing the respective PDN [1, 10].

A. Sdff With And Logic:

The data input in semi dynamic flip-flop is replaced with an AND logic as shown in fig 4. If A=1 and B=0 then the output of SDFF is QB=0.If A=1 and B=1 then QB=1.

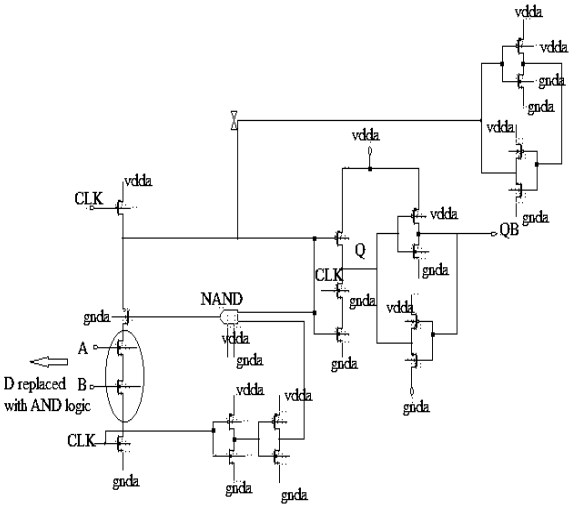

Fig 4: SDFF with AND logic

B. Sdff With Or Logic:

The data input in semi dynamic flip-flop is replaced with an OR logic as shown in fig 5. If A=1 and B=0 then the output of SDFF is QB=1.If A=1 and B=1 then QB=1.

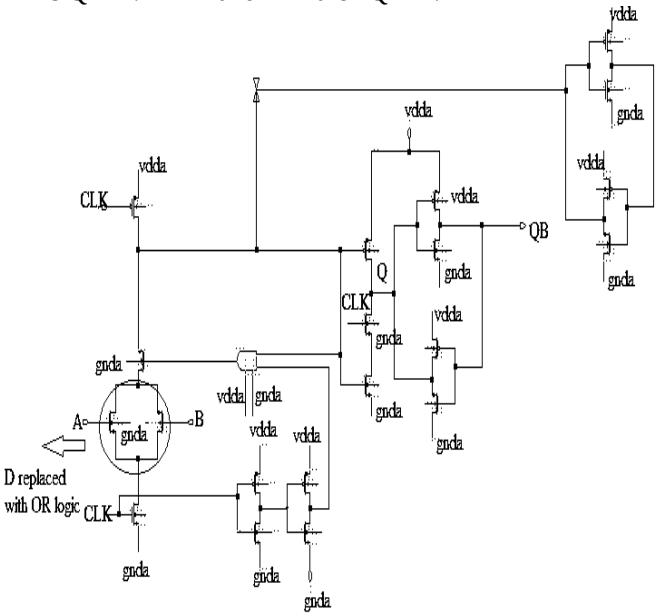

Fig 5: SDFF with OR logic

C. Sdff With Mux Logic:

The data input in semi dynamic flip-flop is replaced with an OR logic as shown in fig 6. If A=1, SEL-A=0 and B=1, SEL-B=1 then the output of SDFF (A.SELA+B.SELB) =1.

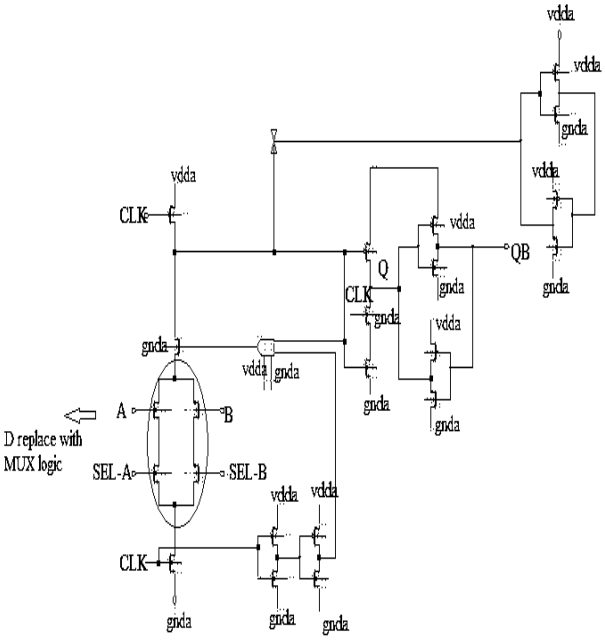

Fig 6: SDFF with MUX logic

D. Ddff With No Elm:

Initially no logic is embedded into DDFF design simply it works as a D-flip flop as shown in fig 7.

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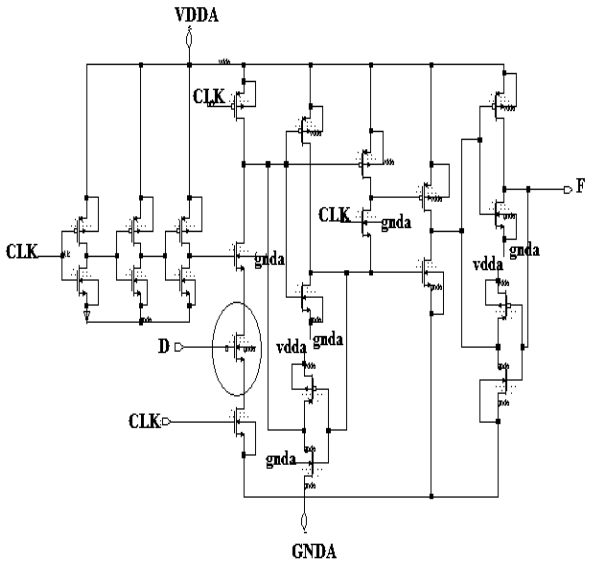

Fig 7: DDFF with no ELM.

E. Ddff With And Logic:

The data input in dual dynamic flip-flop is replaced with an AND logic as shown in fig 8. If A=0 and B=0 then the output of DDFF is Q=0.If A=1 and B=1 then Q=1.

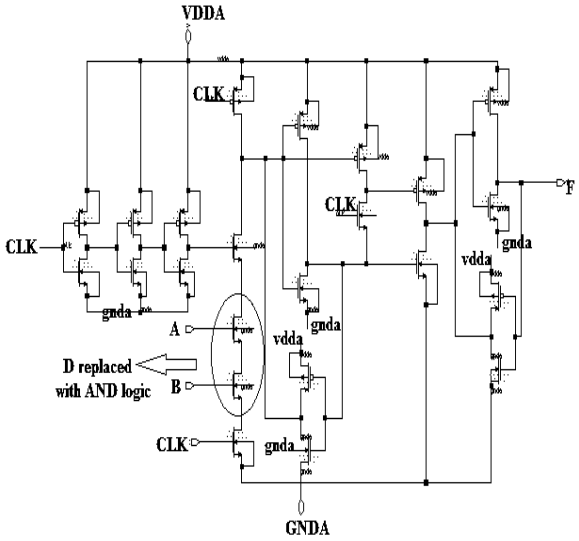

Fig 8: DDFF with AND logic

F. Ddff With Or Logic:

The data input in dual dynamic flip-flop is replaced with an OR logic as shown in fig 9. If A=1 and B=0 then the output of DDFF is Q=1.If A=1 and B=1 then Q=1.

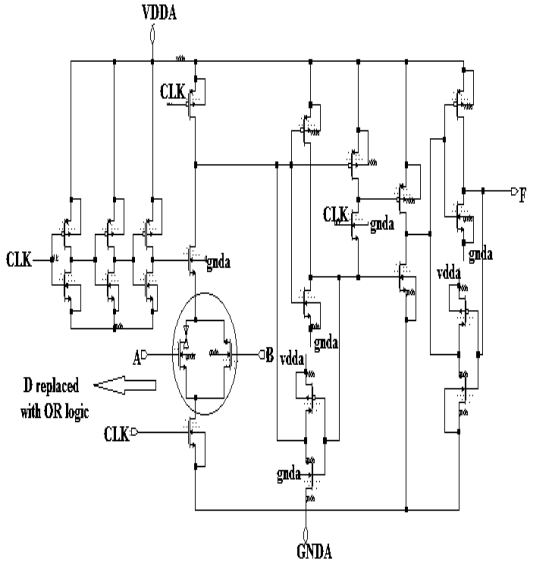

Fig 9: DDFF with OR logic

G. Ddff With Mux Logic:

The data input in dual dynamic flip-flop is replaced with an OR logic as shown in fig 10. If A=1, SEL-A=0 and B=1, SEL-B=1 then the output of DDFF (A.SELA+B.SELB)=1.

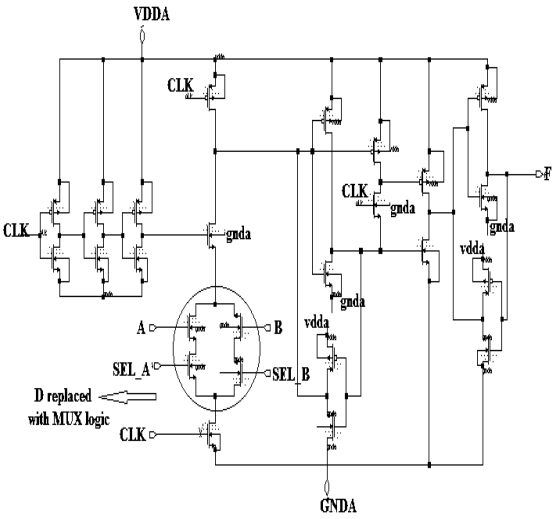

Fig 10: DDFF with MUX logic

H. Proposed Flip-Flop With And Logic:

The data input in proposed flip-flop is replaced with an AND logic as shown in fig 11. If A=0 and B=0 then the output of PFF is Q=0. If A=1 and B=1 then Q=1.

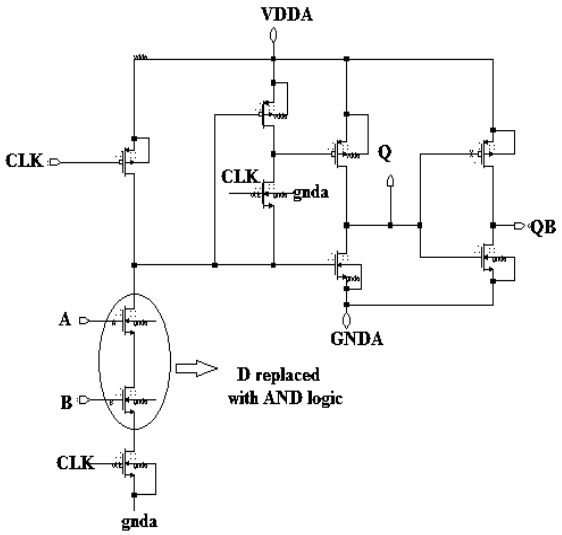

Fig 11: proposed flip flop with AND logic.

I. Proposed Flip-Flop With Or Logic:

The data input in proposed flip-flop is replaced with an OR logic as shown in fig 12. If A=1 and B=0 then the output of PFF is Q=1.If A=1 and B=1 then Q=1.

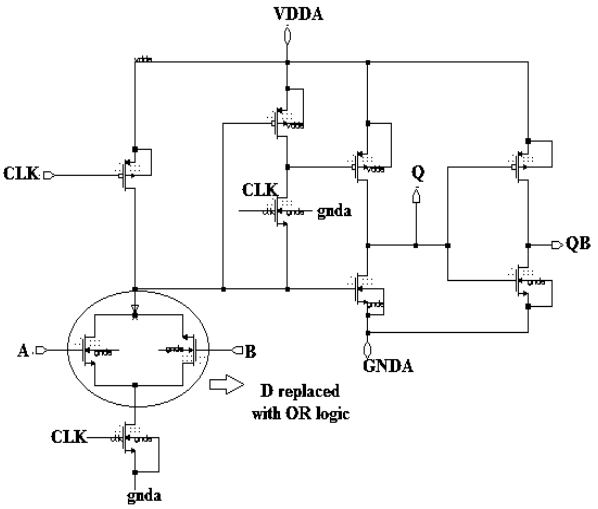

Fig 12: proposed flip flop with OR logic.

J. Proposed Flip-Flop With Mux Logic:

The data input in proposed flip-flop is replaced with an OR logic as shown in fig 13. If A=1, SEL-A=0 and B=1, SEL-B=1 then the output of DDFF (A.SELA+B.SELB) =1.

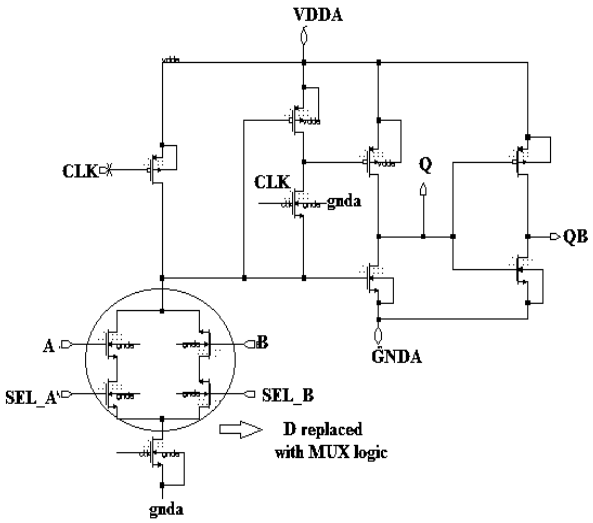

Fig 13: proposed flip flop with MUX logic.

V. Design Of Serial-In Parallel-Out

(Sipo) Shift Register

In Serial-in Parallel-out (SIPO) shift register. The four data bits will be shifted in from "data in" by four clock pulses and is available at q0 through q3. After the first clock, the data at "data in" appears at q0. After the second clock, the old q0 data appears at q1; q0 receives next data from "data in". After the third clock, q1 data is at q2. After the fourth clock, q2 data is at q3. This stage contains the data first present at "data in". The shift register should now contain four data bits.

Fig 14 shows the implementation of SIPO shift register with Dual Dynamic Flip-Flop (DDFF). Fig 15 shows the implementation of SIPO shift register with proposed flip-flop.

VI. Simulation Results

In order to compare the performance of proposed flip-flop with existing flip-flop designs, all the circuits are implemented using Mentor graphics schematic and layout editor and extracted using 130nm CMOS technology. Simulations are carried out using ELDO, with the capacitances and resistances extracted from the layout. These flip-flops are simulated with 2GHz frequency and at 27^0C and the supply voltage of 1.2V. Table I

illustrates the performance comparison of various flip-flops. Table II illustrates the performance comparison of various flip-flops with embedded logic module and table III summarizes comparisons of SIPO shift register.

The simulation waveforms of proposed flip-flop and SIPO shift register is shown in fig 16 and fig 17 respectively.

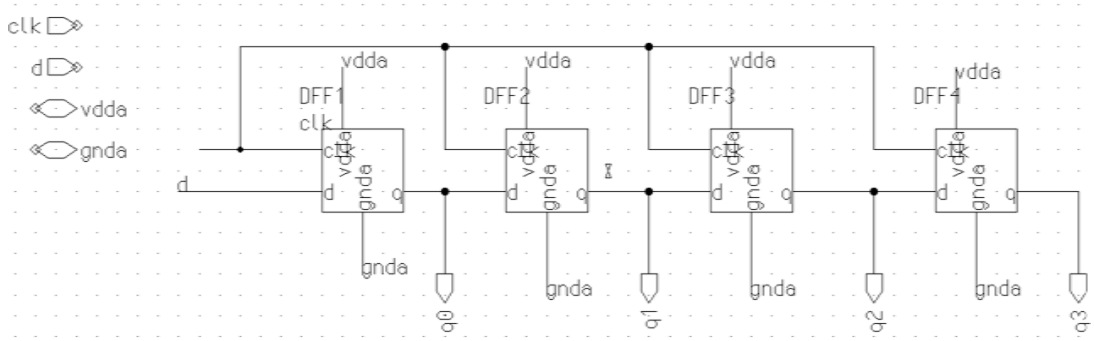

Fig 14: Serial-In Parallel-Out (SIPO) shift register using DDFF.

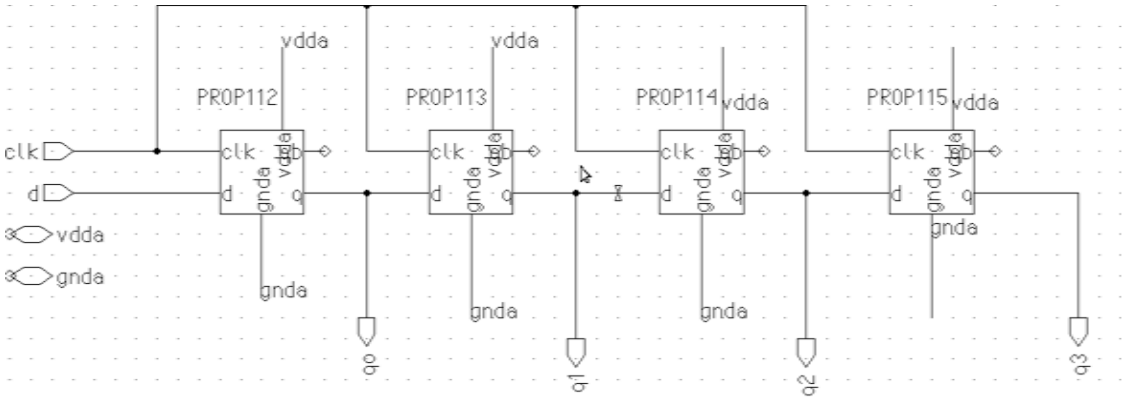

Fig 15: Serial-In Parallel-Out (SIPO) shift register using proposed flip-flop.

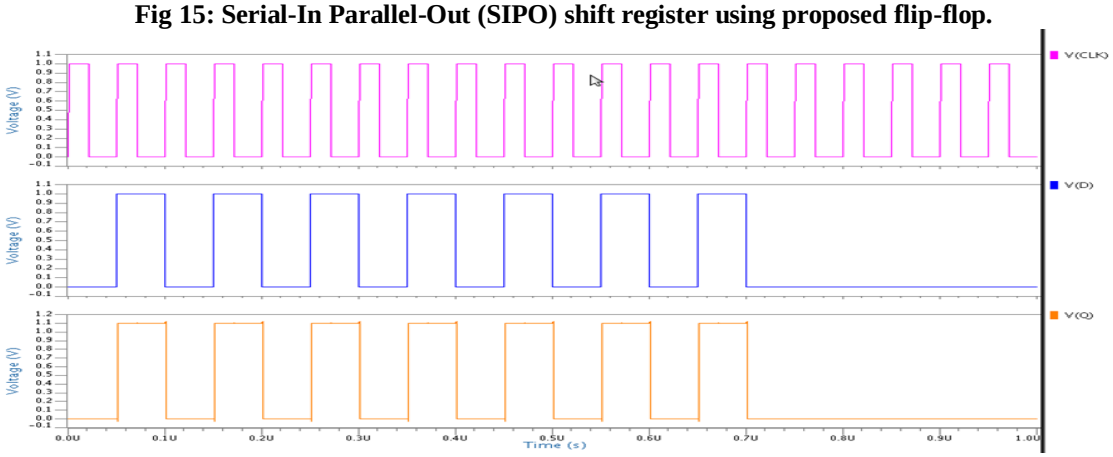

Fig 16: Waveform of proposed flip-flop

Table I: Illustrates The Performance Comparison Of Various Flip-Flops

Flip-Flop	Number of transistors	Total layout area (μm2)	D-Q DELAY	CLK-Q DELAY	RISETIME	FALLTIME	POWER DISSIPATION
SDFF	23	3284.903	50.818ns	163.26ps	64.282ps	22.485ps	67.0844UW
DDFF	18	800.565	274.17ps	660.31ps	155.06ps	231.45ps	14.77NW
Proposed Flip-Flop	10	383.578	238.43ps	350.21ps	113.46ps	144.46ps	6.4889NW

Table Ii: Performance Comparison Of Various Flip-Flops With Embedded Logic Module

Flip-Flop	Number of transistors	Total layout area (μm2)	Width (μm)	CLK-Q DELAY	RISETIME	FALLTIME	POWER DISSIPATION
SDFF OR embedded	24	3289.03	25.263	163.32ps	24.499ps	24.499ps	67.087UW
SDFF AND embedded	24	3310.07	27.562	163.31ps	27.718ps	64.240ps	67.083UW
SDFF MUX embedded	26	3355.60	32.502	163.34ps	26.472ps	64.193ps	67.087UW
DDFF NO ELM	22	1045.91	19.260	161.01ps	31.057ps	37.057ps	15.387NW
DDFF OR embedded	23	1155.01	19.555	165.85ps	29.736ps	32.235ps	15.607NW
DDFF AND embedded	23	1365.76	20.020	189.91ps	30.854ps	38.003ps	14.925NW
DDFF MUX embedded	25	1308.36	23.065	179.74ps	31.073ps	33.708ps	15.108NW
Proposed Flip-Flop OR embedded	10	478.80	10.50	598.77ps	199.57ps.	76.335ps.	6.550NW
Proposed Flip-Flop AND embedded	10	427.55	9.565	362.50ps	119.54ps.	83.307ps	6.050NW
Proposed Flip-Flop MUX embedded	12	635.81	12.710	349.69ps	131.98ps.	87.824ps.	6.5589NW

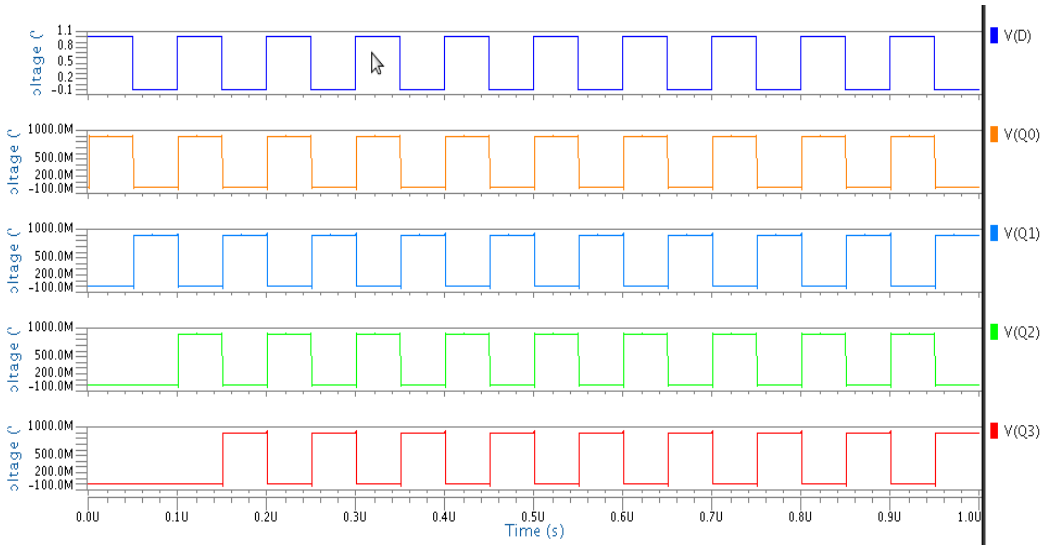

Fig 17: Wave form of SIPO shift register by using proposed flip-flop

Table Iii: Results Of Siso And Sipo Shift Registers

	Technology	**CLK-Q DELAY**	**RISETIME**	**FALLTIME**	**POWER DISSIPATION**
SIPO (DDFF)	130nm	251.65ps	37.710ps	37.743ps	39.1917NW
SIPO (proposed flip-flop)	130nm	408.14ps	156.75ps	103.36ps	29.498NW

VII. Conclusion

A new low power and area efficient flip-flop with embedded logic module is proposed. A comparison of the proposed flip-flop with the conventional flip-flops showed that it exhibits lower power dissipation and occupies less area. The proposed Flip-Flop architecture exhibits reduction in the power dissipation up to 50-60% than the conventional flip-flops. A SIPO shift register is designed using conventional and proposed Flip- Flops. The SIPO shift register designed with proposed flip-flop exhibits reduction in the power dissipation. Hence the proposed architecture is well suited for modern high performance designs where area and power dissipation are the major concern.

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